

Fig - 1A, A New 6-T nMOS Dual Port SRAM

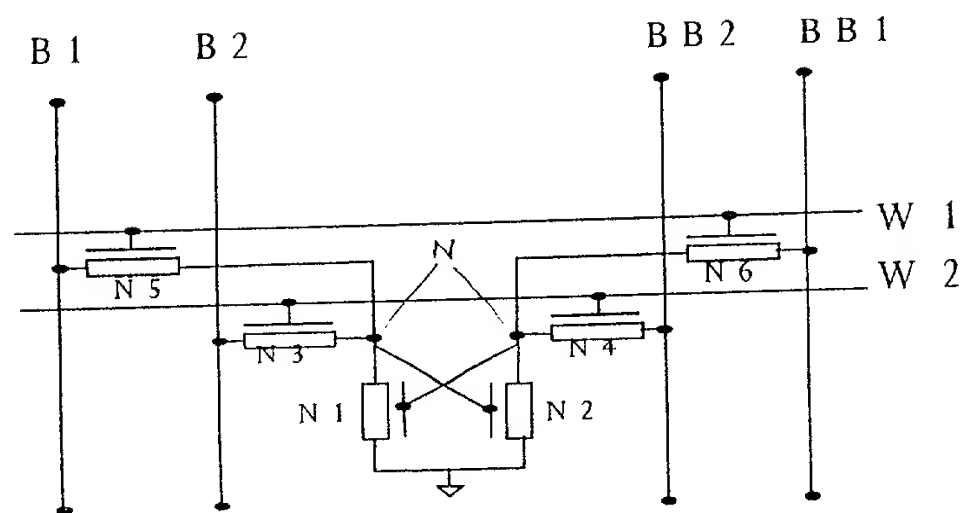
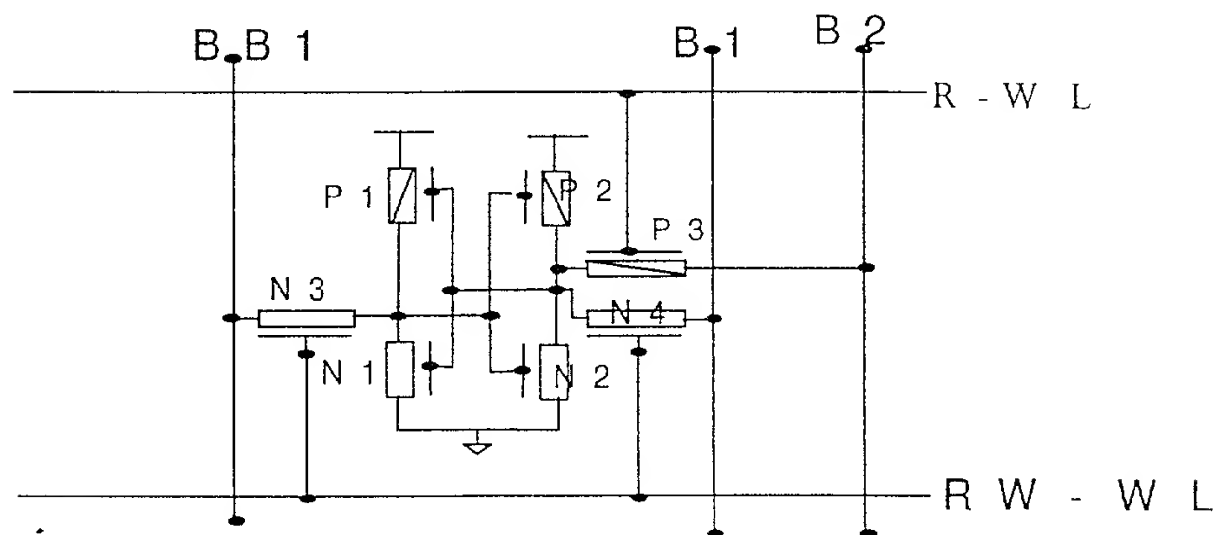
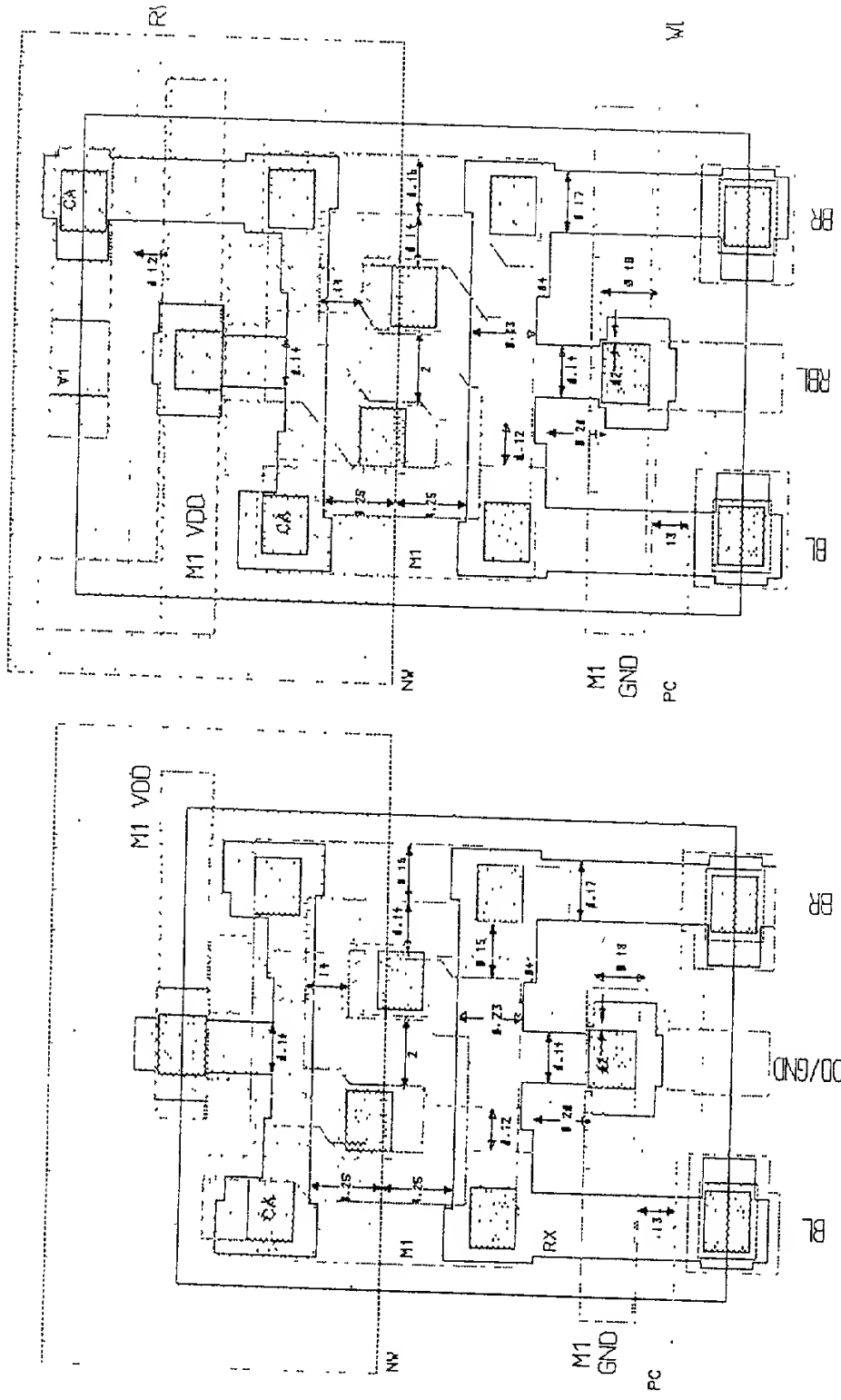


Fig. 1 B , A New 7-T Dual Port SRAM



upper portion of the circuit is a 1T1C1R1 structure, and the lower portion is a 1T1C1R1 structure. The circuit is a 1T1C1R1 structure, and the lower portion is a 1T1C1R1 structure.



1 Port SRAM Cell
1.3 X 1.9 = 2.47
(PRIOR ART)

2 Port SRAM Cell
1.3 X 2.3 = 2.99 (1.22 X 2.47)

Fig. 1C

Fig.2 Dual-Port RAM, Interleave^d Write Operation

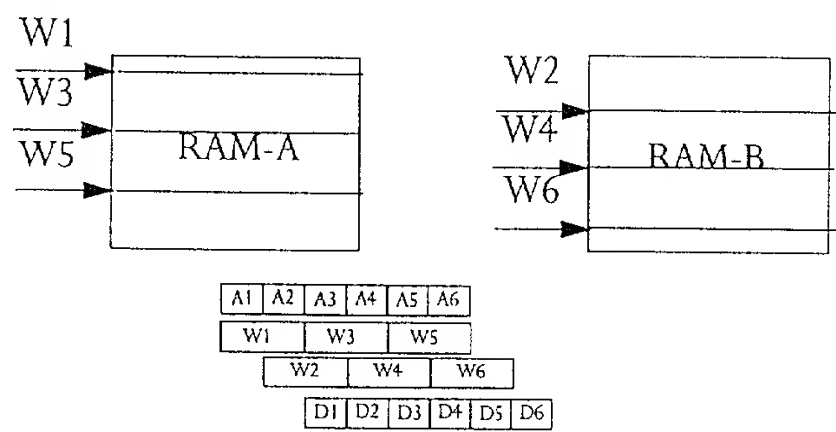


Fig.3 Dual-Port RAM, Interleave^d Read Operation

